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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	2687.3US (94-305.3)
First Inventor or Application Identifier	Walter L. Moden
Title	FLIP CHIP ADAPTOR PACKAGE FOR BARE DIE
Express Mail Label No.	EL638949048US

JC926 U.S. PTO 09/699527 10/30/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original, and a duplicate for fee processing)
2. [X] Specification [Total Pages 22] (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 U.S.C. 113) [Total Sheets 3]
4. Oath or Declaration [Total Pages 1]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 17 completed) **[Note Box 5 below]**
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).
5. [X] Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program (Appendix)
7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 C.F.R.§3.73(b) Statement (when there is an assignee) [ ] Power of Attorney
10. [ ] English Translation Document (if applicable)
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. [ ] * Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. [X] Other: Associate Power of Attorney (37 C.F.R. § 1.34(b))

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon

17. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No 09 / 483,483

Prior application information. Examiner J. Clark Group / Art Unit. 2815

18. CORRESPONDENCE ADDRESS

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Signature	James R. Duzan	Date	11/01/2000

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FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 1,970.00

Complete if Known	
Application Number	Not yet assigned
Filing Date	November 1, 2000
First Named Inventor	Walter L. Moden
Examiner Name	Unknown
Group Art Unit	Unknown
Attorney Docket No.	2687.3US (94-305.3)

METHOD OF PAYMENT

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:
   - Deposit Account Number: 20-1469
   - Deposit Account Name: Trask Britt
   - [ ] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17
   - [ ] Applicant claims small entity status. See 37 CFR 1.27
2. [X] **Payment Enclosed:** [X] Check [ ] Credit card [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	710
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below	Fee Paid
Total Claims	50	-20** =	30	X	18	= 540
Independent Claims	12	- 3** =	9	X	80	= 720
Multiple Dependent					0	= 0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 1,260

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) - 0 -

SUBMITTED BY

Complete (if applicable)

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Signature	James R Duzan			Date	11/01/2000

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PATENT
Attorney Docket 2687.3US (94-305.3)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL638949048US

Date of Deposit with USPS: November 1, 2000

Person making Deposit: Amanda Trulson

APPLICATION FOR LETTERS PATENT

for

FLIP CHIP ADAPTOR PACKAGE FOR BARE DIE

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FLIP CHIP ADAPTOR PACKAGE FOR BARE DIE

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a divisional of application Serial No. 09/483,483, filed January 14, 2000, pending, which is a continuation of application Serial No. 08/948,936, filed October 10, 1997, pending, which is a continuation of application Serial No. 08/574,662, filed December 19, 1995, now U.S. Patent 5,719,440, issued February 17, 1998.

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to an apparatus for connecting a bare semiconductor die having a size and bond pad arrangement, either solder ball arrangement, or pin arrangement (hereinafter referred to generally as a "terminal arrangement"), which does not conform to a printed circuit board with a specific or standardized pin out, connector pad, or lead placement (hereinafter referred to generally as a "connection arrangement"). More particularly, the present invention relates to an intermediate conductor-carrying substrate (hereinafter referred to generally as an "adaptor board") for connecting a non-conforming bare die to another printed circuit board having a given connection arrangement (hereinafter referred to generally as a "master board").

State of the Art: Definitions: The following terms and acronyms will be used throughout the application and are defined as follows:

BGA - Ball Grid Array: An array of minute solder balls disposed on an attachment surface of a semiconductor die wherein the solder balls are refluxed for simultaneous attachment and electrical communication of the semiconductor die to a printed circuit board.

COB - Chip On Board: The techniques used to attach semiconductor dice to a printed circuit board, including flip chip attachment, wirebonding, and tape automated bonding ("TAB").

Flip Chip: A chip or die that has bumped terminations spaced around the active surface of the die and is intended for facedown mounting.

Flip Chip Attachment: A method of attaching a semiconductor die to a substrate in which the die is flipped so that the connecting conductor pads on the face of the die are set on mirror-image pads on the substrate (i.e. printed circuit board) and bonded by refluxing the solder.

Glob Top: A glob of encapsulant material (usually epoxy or silicone or a combination thereof) surrounding a semiconductor die in the COB assembly process.

PGA - Pin Grid Array: An array of small pins extending substantially perpendicularly from the major plane of a semiconductor die, wherein the pins conform to a specific arrangement on a printed circuit board for attachment thereto.

SLICC - Slightly Larger than Integrated Circuit Carrier: An array of minute solder balls disposed on an attachment surface of a semiconductor die similar to a BGA, but having a smaller solder ball pitch and diameter than a BGA.

* * * * *

State-of-the-art COB technology generally consists of three semiconductor dies to printed circuit boards attachment techniques: flip chip attachment, wirebonding, and TAB.

Flip chip attachment consists of attaching a semiconductor die, generally having a BGA, a SLICC or a PGA, to a printed circuit board. With the BGA or SLICC, the solder ball arrangement on the semiconductor die must be a mirror-image of the connecting bond pads on the printed circuit board such that precise connection is made. The semiconductor die is bonded to the printed circuit board by refluxing the solder balls. With the PGA, the pin arrangement of the semiconductor die must be a mirror-image of the pin recesses on the printed circuit board. After insertion, the semiconductor die is generally bonded by soldering the pins into place. An under-fill encapsulant is generally disposed between the semiconductor die and the printed circuit board to prevent contamination. A variation of the pin-in-recess PGA is a J-lead PGA, wherein the loops

of the J's are soldered to pads on the surface of the circuit board. Nonetheless, the lead and pad locations must coincide, as with the other referenced flip-chip techniques.

Wirebonding and TAB attachment generally begins with attaching a semiconductor die to the surface of a printed circuit board with an appropriate adhesive. In wirebonding, a plurality of bond wires are attached, one at a time, from each bond pad on the semiconductor die and to a corresponding lead on the printed circuit board. The bond wires are generally attached through one of three industry-standard wirebonding techniques: ultrasonic bonding - using a combination of pressure and ultrasonic vibration bursts to form a metallurgical cold weld; thermocompression bonding - using a combination of pressure and elevated temperature to form a weld; and thermosonic bonding - using a combination of pressure, elevated temperature, and ultrasonic vibration bursts. The die may be oriented either face up or face down (with its active surface and bond pads either up or down with respect to the circuit board) for wire bonding, although face up orientation is more common. With TAB, metal tape leads are attached between the bond pads on the semiconductor die and the leads on the printed circuit board. An encapsulant is generally used to cover the bond wires and metal tape leads to prevent contamination.

Although the foregoing methods are effective for bonding semiconductor dies to printed circuit boards, the terminal arrangements of the dies and the connection arrangements of the boards must be designed to accommodate one another. Thus, it may be impossible to electrically connect a particular semiconductor die to a printed circuit board for which the semiconductor die terminal arrangement was not designed to match the board's connection arrangement. With either wirebond or TAB attachment, the semiconductor die bond pad may not correspond to the lead ends on the circuit board, and thus attachment is either impossible or extremely difficult due to the need for overlong wires and the potential for inter-wire contact and shorting. With flip chip attachment, if the printed circuit board connection arrangement is not a mirror-image of the solder ball or pin arrangement (terminal arrangement) on the semiconductor die, electrically connecting the flip chip to the printed circuit board is impossible.

Therefore, it would be advantageous to develop an apparatus for connecting a semiconductor die having a size and bond pad arrangement, solder ball arrangement, or pin arrangement ("I/O pattern") which does not conform to a printed circuit board with a specific or standardized pin out, connection pad location, or lead placement ("I/O pattern").

BRIEF SUMMARY OF THE INVENTION

The present invention relates to an intermediate printed circuit board or other conductor-carrying substrate that functions as an adaptor board for electrically connecting one or more bare semiconductor dies of a variety of sizes and bond pad locations, solder ball arrangement, or pin arrangement, to a master printed circuit board with a specific or standardized pin out, connector pad location, or lead placement.

An adaptor printed circuit board or substrate ("adaptor board") is sized and configured with an I/O pattern to accommodate its attachment to the master printed circuit board ("master board"). If the master board is configured to receive a specific pin out or specific connector pad locations, the adaptor board is configured on its master board attachment surface with pins or solder balls in mirror-image to the master board connection arrangement to make electrical contact with the specific pin out or connector pads on the printed circuit board. If the master board is configured to receive a bond wire, the adaptor board is configured and sized to provide wire bond pads on its upper surface closely adjacent the bond pads of the master board leads. The adaptor board can, of course, be configured to accommodate other attachment and electrical connection means known in the industry, as well as other components in addition to the semiconductor die or dice carried thereon.

On the semiconductor die side of the adaptor board, one or more semiconductor dies are attached. If a "flip chip" die is attached to the adaptor board, the adaptor board will, of course, be configured with an I/O pattern to receive the flip chip with a specific pin out or connector pad locations. The pin out or connector pads on the adaptor board are connected to circuit traces on or through the adaptor board. The circuit traces form

the electrical communication path from the pin recesses or connector pads on the adaptor board to the connection points to the master board.

If a "leads over" die is used with the adaptor board, the bond pads on the die are wirebonded to the adaptor board. Preferably, the leads over die is attached to the adaptor board with the bond pads facing the adaptor board. The bond wires are attached to the leads over die bond pads and extend into a via or vias in the adaptor board. The bond wires are attached to an I/O pattern of adaptor board bond pads within the via from which circuit traces extend, or to leads on the master board side of the adaptor board.

It is, of course, understood that the leads over die can be attached to the adaptor board with the bond pads facing away from the adaptor board. Thus, the bond wires are simply attached to the bond pads on the leads over die and to a corresponding I/O pattern of adaptor board pad on the semiconductor die side of the adaptor board.

Preferably, the exposed circuitry of the die and the die-to-adaptor board interconnection is sealed from contamination by a glob top after wire bonding or an underflow compound in the case of a flip chip attach.

Furthermore, it is understood that with the use of wire bonds, the adaptor boards can be stacked on top of each other and connected to the adaptor board as by wire bonding.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIG. 1 is a side view of one embodiment of the present invention;

FIG. 2 is a side view of a second embodiment of the present invention;

FIG. 2A is a top view of the second embodiment of the present invention shown in FIG. 2;

FIG. 3 is a side view of a third embodiment of the present invention; and

FIG. 4 is a side view of a fourth embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 illustrates a first embodiment of the present invention designated as a flip chip style/flip chip attach assembly 100. Assembly 100 comprises a semiconductor die 12 having an inverted active surface 14 with at least one flip chip electric connection 16 (such as a C4 solder bump connection, a pin connection, or a surface mount j-lead connection, by way of example) extending substantially perpendicularly from a bond pad 15 on the semiconductor die surface 14. The flip chip electric connections 16 are attached to an upper surface 20 of an adaptor board 18 in such a manner that the flip chip electric connections 16 make electrical contact with electrical contact elements 21 in or on the surface of adaptor board 18. The electrical contact elements 21 make electrical communication between each flip chip electric connection 16, through circuit traces 23 (exemplary traces shown in broken lines) in the adaptor board 18, to at least one master board connector 22 extending substantially perpendicularly from a lower surface 24 of the adaptor board 18 to connect adaptor board 18 to an aligned terminal 31 on master board 30. Preferably, a sealing compound 26 is disposed between the semiconductor die 12 and the adaptor board 18 to prevent contamination of the die-to-adaptor board connections 16 and to more firmly secure die 12 to adaptor board 18.

In actual practice, there will be a plurality of terminals 31 arranged in a specific, perhaps industry-standard pattern, on master board 30, and master board connectors will be arranged in a mirror-image pattern to terminals 31 for mating connection therewith. Master board connectors 22 and terminals 31 may comprise any electrical connection mechanism known in the art, in addition to those previously described herein.

FIGS. 2 and 2A illustrate a second embodiment of the present invention designated as a flip chip style/wire bond attach assembly 200. Components common to both FIG. 1 and FIG. 2 retain the same numeric designation. The assembly 200 comprises the semiconductor die 12 having lower surface 14 with at least one flip chip

electric connection 16, as known in the art, extending substantially perpendicularly from a bond pad 15 on the semiconductor die lower surface 14. The flip chip electric connections 16 are attached to the adaptor board upper surface 20 in such a manner that the flip chip electric connections 16 make electrical contact with electrical contact elements 21 on the adaptor board 18. The electrical contact elements 21 communicate between each flip chip electric connection 16 to bond pads 28 on the adaptor board upper surface 20 through circuit traces 23. The adaptor board lower surface 24 is bonded to an upper surface 36 of a master board 30 with an adhesive 32, which may comprise a liquid or gel adhesive, or an adhesive tape, all as known in the art. If desired, adhesive 32 may be a heat-conductive adhesive. A wire bond 34 extends from each adaptor board bond pad 28 to a corresponding bond pad or lead end 35 on the upper surface 36 of master board 30, bond pad or lead end 35 communicating with other components mounted to master board 30 or with other components on other boards or other assemblies through circuit traces or other conductors known in the art.

FIG. 3 illustrates a third embodiment of the present invention designated as a wire bond style/flip chip attach assembly 300. Components which are common to the previous figures retain the same numeric designation. The assembly 300 comprises an inverted semiconductor die 12 having lower surface 14 with at least one bond pad 38 on the semiconductor die lower surface 14. As illustrated, the bond pads 38 are arranged in two rows extending down the longitudinal axis of die 12 being located transverse to the plane of the page, such an arrangement commonly being used for a "leads over" connection to frame leads extending over the die in its normal, upright position. The semiconductor die lower surface 14 is bonded to the adaptor board upper surface 20 with an insulating, sealing adhesive 40. The adaptor board 18 includes at least one wire bond via 42 which is located in a position or positions aligned with the semiconductor die bond pads 38. Each individual wire bond 134 is connected to each corresponding individual semiconductor die bond pad 38. Each wire bond 134 extends from the semiconductor die bond pad 38 to a corresponding bond pad or lead 39 on the adaptor board lower surface 24, which communicates with adaptor board connectors 22 through circuit

traces 23. The master board terminals 31 are in electrical communication with at least one adaptor board connector 22 extending substantially perpendicularly from the adapter board lower surface 24. Preferably, a sealant 44 encases the bond wires 134 and seals the wire bond via 42 to prevent contamination and damage to the wire bonds.

FIG. 4 illustrates a fourth embodiment of the present invention designated as a wire bond style/wire bond attach assembly 400. Components which are common to the previous figures retain the same numeric designation. The assembly 400 comprises the semiconductor die 12 having lower surface 14 with at least one bond pad 38 on the semiconductor die lower surface 14. As with the embodiment of FIG. 3, die 12 in this instance employs bond pads 38 in a "leads over" configuration. The semiconductor die lower surface 14 is bonded to the adaptor board upper surface 20 with an insulating, sealing adhesive 40. The adaptor board 18 includes at least one wire bond via 42 which is located in a position or positions aligned with the semiconductor die bond pads 38. Each individual wire bond 134 is connected to each corresponding semiconductor die bond pad 38. Each wire bond 134 extends from the semiconductor die bond pad 38 to a corresponding bond pad 46 within the wire bond via 42. The via bond pads 46 are in electrical communication through circuit traces 23 with at least one corresponding adapter board bond pad 28. The adaptor board lower surface 24 is bonded to the master board upper surface 36 with the adhesive 32. Wire bonds 34 extend from the adapter board upper surface 20 to a corresponding bond pad or lead on the master board upper surface 36. Preferably, the wire bond via sealant 44 encases the bond wires 134 and seals the wire bond via 42 to prevent contamination.

* * * * *

Having thus described in detail preferred embodiments of the present invention, it is to be understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A method of electrically connecting a semiconductor die to a substrate, comprising:

providing a semiconductor die having a surface having a plurality of bond pads thereon;

providing a substrate having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board;

attaching the surface having a plurality of bond pads thereon of the semiconductor die to the die side surface of said board; and

connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through said at least one via extending through said board

2. The method of claim 1, further comprising:

applying an adhesive to a portion of the die side of the substrate to attach the semiconductor die thereto.

3. The method of claim 1, further comprising:

filling at least a portion of the via in the substrate with a sealant.

4. The method of claim 1, further comprising:

filling the via in the substrate with a sealant.

5. A method of electrically connecting a semiconductor die to a master board, comprising:

providing a semiconductor die having a plurality of bond pads thereon;

providing a master board having a plurality of circuit traces thereon;

providing a board having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board;

providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board;

attaching said semiconductor die to a portion of the die side surface of the board;

connecting said plurality of bond pads of said semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the at least one via extending through then board; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board.

6. The method of claim 5, wherein the board includes a plurality of vias extending therethrough.

7. The method of claim 5, wherein the plurality of electrical connectors comprise solder balls.

8. A method of electrically connecting at least two semiconductor die to a substrate, comprising:

providing at least two semiconductor die, each semiconductor die having a surface having a plurality of bond pads thereon;

providing a substrate having a die side surface, a second attachment surface, at least two vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board;

attaching the surface having a plurality of bond pads thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the board having the plurality of bond pads of the semiconductor die located over one of the at least two vias extending through the board ; and

connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the one via extending through the board of the at least two vias extending through the board.

9. The method of claim 8, further comprising:

applying an adhesive to a portion of the die side of the substrate to attach each semiconductor die thereto.

10. The method of claim 8, further comprising:

filling at least a portion of each via in the substrate with a sealant.

11. The method of claim 8, further comprising:

filling each via in the substrate with a sealant.

12. A method of electrically connecting a plurality of semiconductor die to a master board, comprising:

providing a plurality of semiconductor die, each semiconductor die having a plurality of bond pads thereon;

providing a master board having a plurality of circuit traces thereon;

providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board;

providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board;

attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board;

connecting said plurality of bond pads of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the a via extending through then board; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board.

13. The method of claim 12, wherein the plurality of electrical connectors comprise solder balls.

14. The method of claim 12, wherein the plurality of electrical connectors comprise pins.

15. The method of claim 12, further comprising:

filling at least a portion of each via in the board with a sealant.

16. The method of claim 12, further comprising:

filling each via in the board with a sealant.

17. A method of electrically connecting a semiconductor die to a master board, comprising:

providing a semiconductor die having a plurality of bond pads thereon;

providing a master board having a plurality of circuit traces thereon;

providing a board having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment

surface, a plurality of circuits, and a plurality of bond pads located on the die side surface of the board;

providing a plurality of electrical connectors for connecting the plurality of bond pads located on the die side surface of the board to the circuit traces of the master board;

attaching said semiconductor die to a portion of the die side surface of the board;

connecting said plurality of bond pads of said semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the at least one via extending through then board; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board.

18. The method of claim 17, wherein the board includes a plurality of vias extending therethrough.

19. The method of claim 17, wherein the plurality of electrical connectors comprise wire bonds.

20. A method of electrically connecting a plurality of semiconductor die to a master board, comprising:

providing a plurality of semiconductor die, each semiconductor die having a plurality of bond pads thereon;

providing a master board having a plurality of circuit traces thereon;

providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the die side surface of the board;

providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board;

attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board;

connecting said plurality of bond pads of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the a via extending through then board; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board.

21. The method of claim 20, wherein the plurality of electrical connectors comprise wire bonds.

22. The method of claim 20, wherein the plurality of electrical connectors comprise pins.

23. The method of claim 20, further comprising:

filling at least a portion of each via in the board with a sealant.

24. The method of claim 20, further comprising:

filling each via in the board with a sealant.

25. The method of claim 20, further comprising:

applying an adhesive to a portion of the die side surface to attach each semiconductor die thereto.

26. A method of attaching a semiconductor die to a substrate, comprising:

providing a semiconductor die having a surface having at least one bond pads thereon;

providing a substrate having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and at least one bond pad located on the second attachment surface of the board;

attaching the surface having at least one bond pad thereon of the semiconductor die to the die side surface of said board; and

connecting said at least one bond pad of the semiconductor die to said at least one bond pad of said board using at least one wire bond, said at least one wire bond extending through said at least one via extending through said board

27. The method of claim 26, further comprising:

applying an adhesive to a portion of the die side of the substrate to attach the semiconductor die thereto.

28. The method of claim 26, further comprising:

filling at least a portion of the via in the substrate with a sealant.

29. The method of claim 26, further comprising:

filling the via in the substrate with a sealant.

30. A method of attaching a semiconductor die to a master board, comprising:

providing a semiconductor die having at least one bond pad thereon;

providing a master board having at least one circuit trace thereon;

providing a board having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, at least one circuit, and at least one bond pad located on the second attachment surface of the board;

providing at least one electrical connector for connecting the at least one bond pad located on the second attachment surface of the board to the at least one circuit trace of the master board;

attaching said semiconductor die to a portion of the die side surface of the board;

connecting said at least one bond pad of said semiconductor die to said at least one bond pad of said board using at least one wire bond, said at least one wire bond extending through the at least one via extending through then board; and

connecting said board and master board using said at least one electrical connector on said board to said at least one circuit trace on said master board.

31. The method of claim 30, wherein the board includes a plurality of vias extending therethrough.

32. The method of claim 30, wherein the at least one electrical connector comprises at least one solder ball.

33. A method of attaching at least two semiconductor die to a substrate, comprising:

providing at least two semiconductor die, each semiconductor die having a surface having at least one bond pad thereon;

providing a substrate having a die side surface, a second attachment surface, at least two vias extending through the board from the die side surface to the second attachment surface, at least two circuits, and at least two bond pads located on the second attachment surface of the board;

attaching the surface having at least one bond pad thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the board having the at least one bond pad of the semiconductor die located over one of the at least two vias extending through the board ; and

connecting said at least one of each of the semiconductor die to said at least two bond pads of said board using at least two wire bonds, at least one wire bond of said at least two wire bonds extending through the one via extending through the board of the at least two vias extending through the board.

34. The method of claim 33, further comprising:

applying an adhesive to a portion of the die side of the substrate to attach each semiconductor die thereto.

35. The method of claim 33, further comprising:

filling at least a portion of each via in the substrate with a sealant.

36. The method of claim 33, further comprising:

filling each via in the substrate with a sealant.

37. A method of attaching a plurality of semiconductor die to a master board, comprising:

providing a plurality of semiconductor die, each semiconductor die having at least one bond pad thereon;

providing a master board having a plurality of circuit traces thereon;

providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board;

providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board;

attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board;

connecting said at least one bond pad of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the plurality of vias extending through then board; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board.

38. The method of claim 37, wherein the plurality of electrical connectors comprise solder balls.

39. The method of claim 37, wherein the plurality of electrical connectors comprise pins.

40. The method of claim 37, further comprising:

filling at least a portion of each via in the board with a sealant.

41. The method of claim 37, further comprising:

filling each via in the board with a sealant.

42. A method of attaching a semiconductor die to a master board, comprising:

providing a semiconductor die having at least one bond pad thereon;

providing a master board having at least one circuit trace thereon;

providing a board having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, at least one circuit, and at least one bond pad located on the die side surface of the board;

providing at least one electrical connector for connecting the at least one bond pad located on the die side surface of the board to the at least one circuit trace of the master board;

attaching said semiconductor die to a portion of the die side surface of the board;

connecting said at least one bond pad of said semiconductor die to said at least one bond pads of said board using at least one wire bond, said at least one wire bond extending through the at least one via extending through then board; and

connecting said board and master board using said at least one electrical connector on said board to said at least one circuit trace on said master board.

43. The method of claim 42, wherein the board includes a plurality of vias extending therethrough.

44. The method of claim 42, wherein the at least one electrical connector comprises at least one wire bond.

45. A method of attaching a plurality of semiconductor die to a master board, comprising:

providing a plurality of semiconductor die, each semiconductor die having at least one bond pad thereon;

providing a master board having a plurality of circuit traces thereon;

providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the die side surface of the board;

providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board;

attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board;

connecting said at least one bond pad of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, at least one wire bond of said

plurality of wire bonds extending through at least one via of the plurality of vias extending through then board; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board.

46. The method of claim 45, wherein the plurality of electrical connectors comprise wire bonds.

47. The method of claim 45, wherein the plurality of electrical connectors comprise pins.

48. The method of claim 45, further comprising:

filling at least a portion of each via in the board with a sealant.

49. The method of claim 45, further comprising:

filling each via in the board with a sealant.

50. The method of claim 45, further comprising:

applying an adhesive to a portion of the die side surface to attach each semiconductor die thereto.

ABSTRACT OF THE DISCLOSURE

A board for connecting a bare semiconductor die with a bond pad arrangement which does not conform to a master printed circuit board with a specific or standardized pin out, connector pad, or lead placement arrangement. The board comprises a printed circuit board including first elements, such as minute solder balls, pins, or bond wires, for making electrical contact between the board and the master board, and second elements, such as minute solder balls, pins, or bond wires, for making electrical contact between the semiconductor die and the board. The board has circuit traces for electrical communication between the board/master board electrical contact elements, and the semiconductor die board electrical contact elements.

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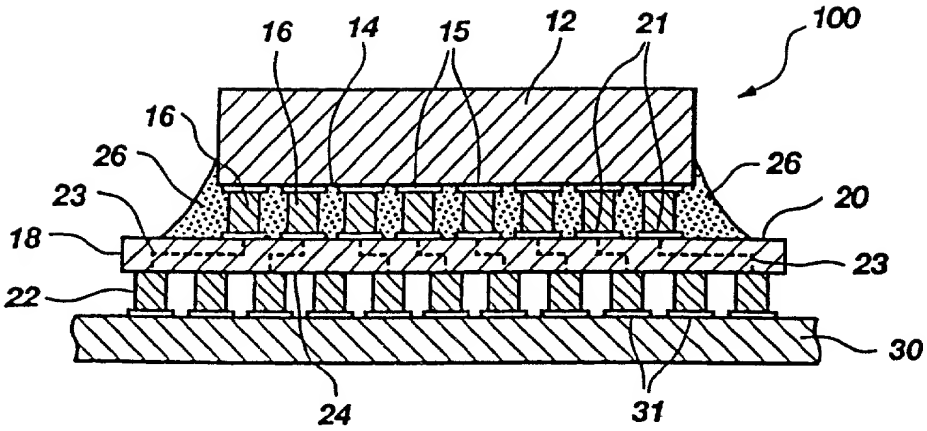
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Fig. 1

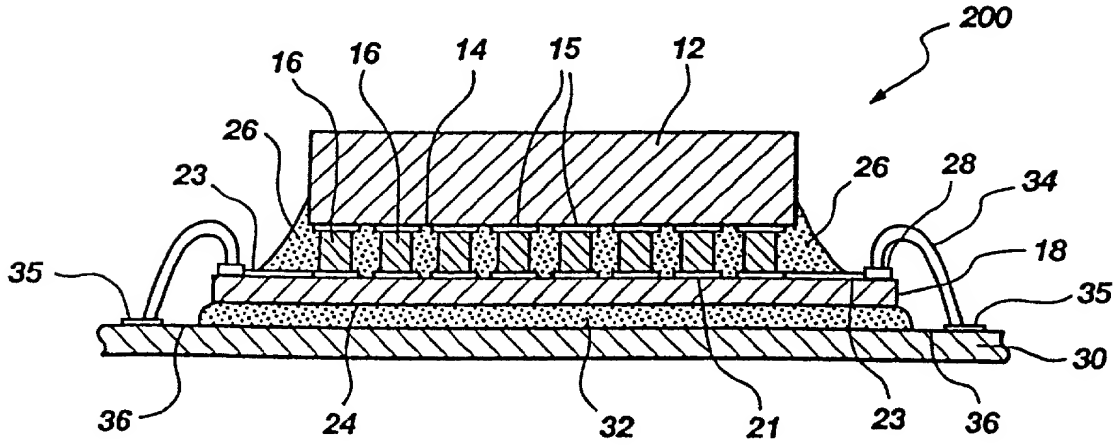
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Fig. 2

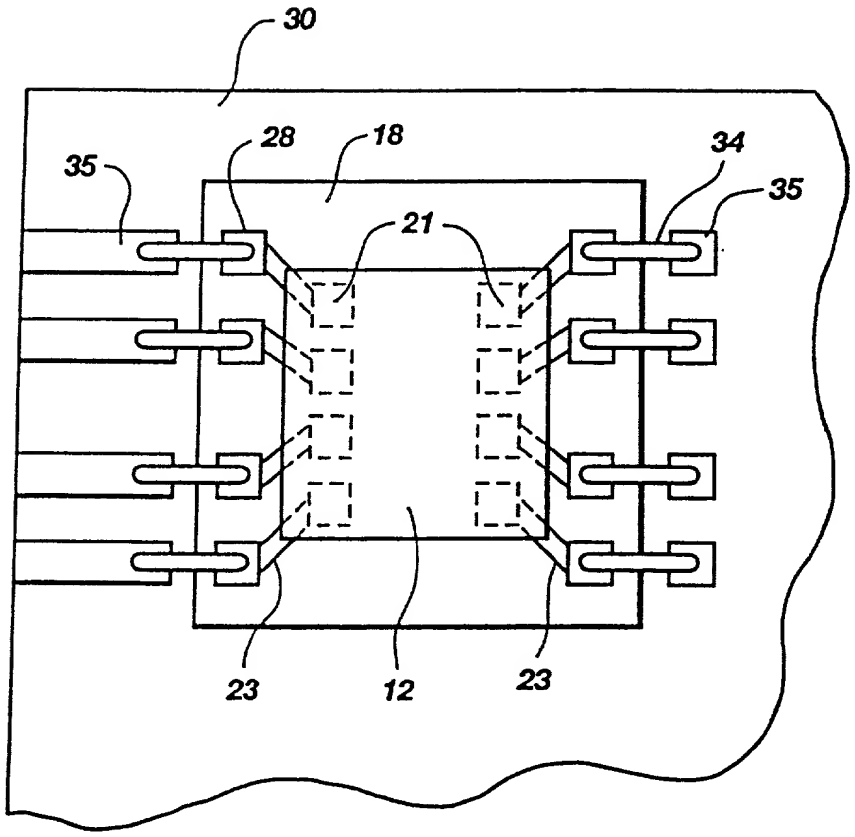

Fig. 2A

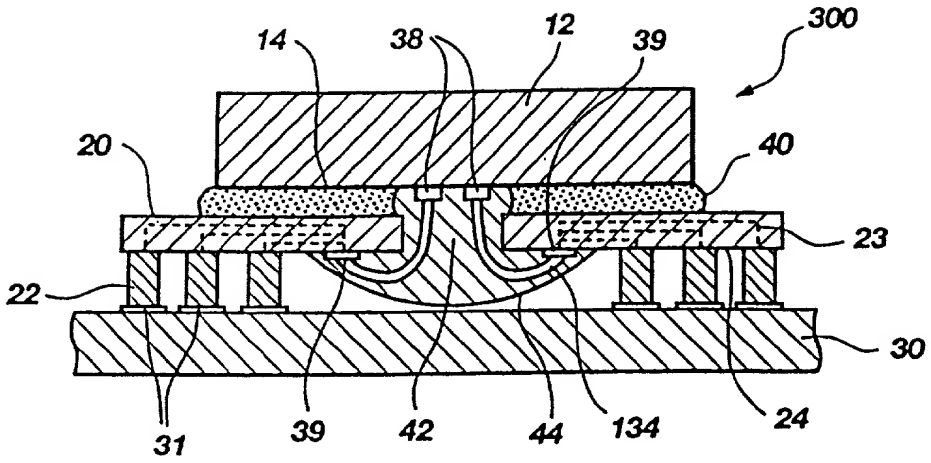
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Fig. 3

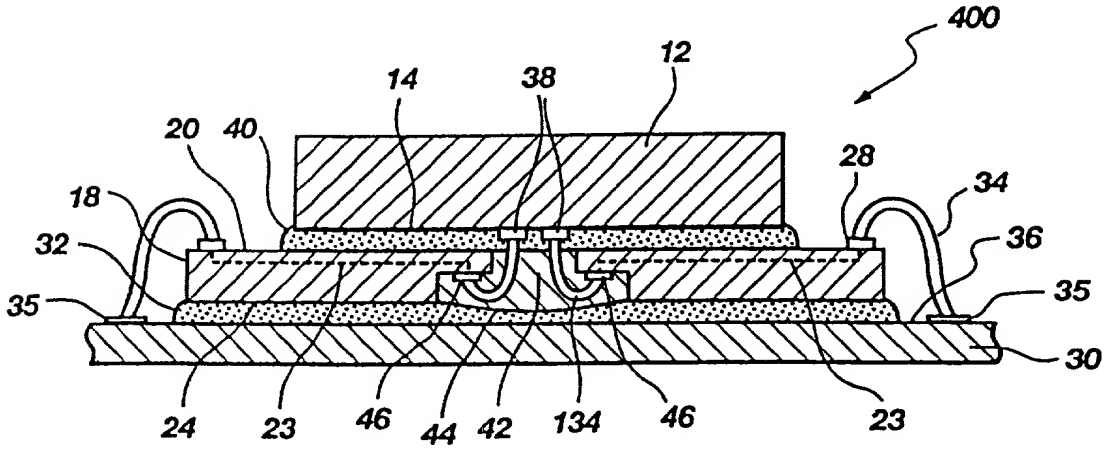
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Fig. 4

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on a[redacted]ched continuation page, I hereby declare that[redacted]
My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **FLIP CHIP ADAPTOR PACKAGE FOR BARE DIE**, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the Untied States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority Claimed	
(number)	(country)	(day/month/year filed)	Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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TRASK, BRITT & ROSSA
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole inventor: Walter L. Moden
Inventor's signature _____ Date 12-18-95
Residence: Meridian, Idaho
Citizenship: U.S.A.
Post Office Address: 622 Woodbury, Meridian, Idaho 83642

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Walter L. Moden

Serial No.: 08/574,662

Filed: December 19, 1995

For: FLIP CHIP ADAPTOR PACKAGE FOR BARE DIE

Examiner: Unknown

Group Art Unit: Unknown

Attorney Docket No.: 2687US

CERTIFICATE OF MAILING

I hereby certify that this paper or fee along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail (under 37 C.F.R. § 1.8(a)) on the date of deposit shown below with sufficient postage and in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

February 27, 1996
Date of Deposit

Stacey Lucero
Signature of registered practitioner or other person having reasonable basis to expect mailing to occur on date of deposit shown pursuant to 37 C.F.R. § 1.8(a)(1)(ii)

Stacey Lucero
Typed/printed name of person whose signature is contained above

ASSOCIATE POWER OF ATTORNEY
(37 C.F.R. § 1.34(b))

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. § 1.34(b), please recognize the following individuals as an associate agent/attorney herein in connection with the above-identified patent application:

W. Bryan Farney, Reg. No. 32,651
Michael L. Lynch, Reg. No. 30,871

Respectfully submitted,

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JRD/sll